IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

YONEMARU, M. Atty. Ref.: 829-618; Confirmation No.

Appl. No. 10/720,764 TC/A.U. 2826

Filed: November 25, 2003 Examiner: Dickey, T.

For: SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT AND FABRICATION METHOD FOR SAME

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December 27, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

AMENDMENT IN RCE

Responsive to the Official Actions dated July 27, 2005 and November 18, 2005, please amend the above-identified application as follows (an RCE has been filed herewith):

AMENDMENTS TO THE TITLE:

Please amend the title as follows:

SEMICONDUCTOR INTEGRATED LOGIC CIRCUIT INCLUDING TWO PMOS TRANSISTORS CONNECTED IN SERIES AND TWO NMOS TRANSISTORS CONNECTED IN SERIES ~~AND FABRICATION METHOD FOR SAME~~